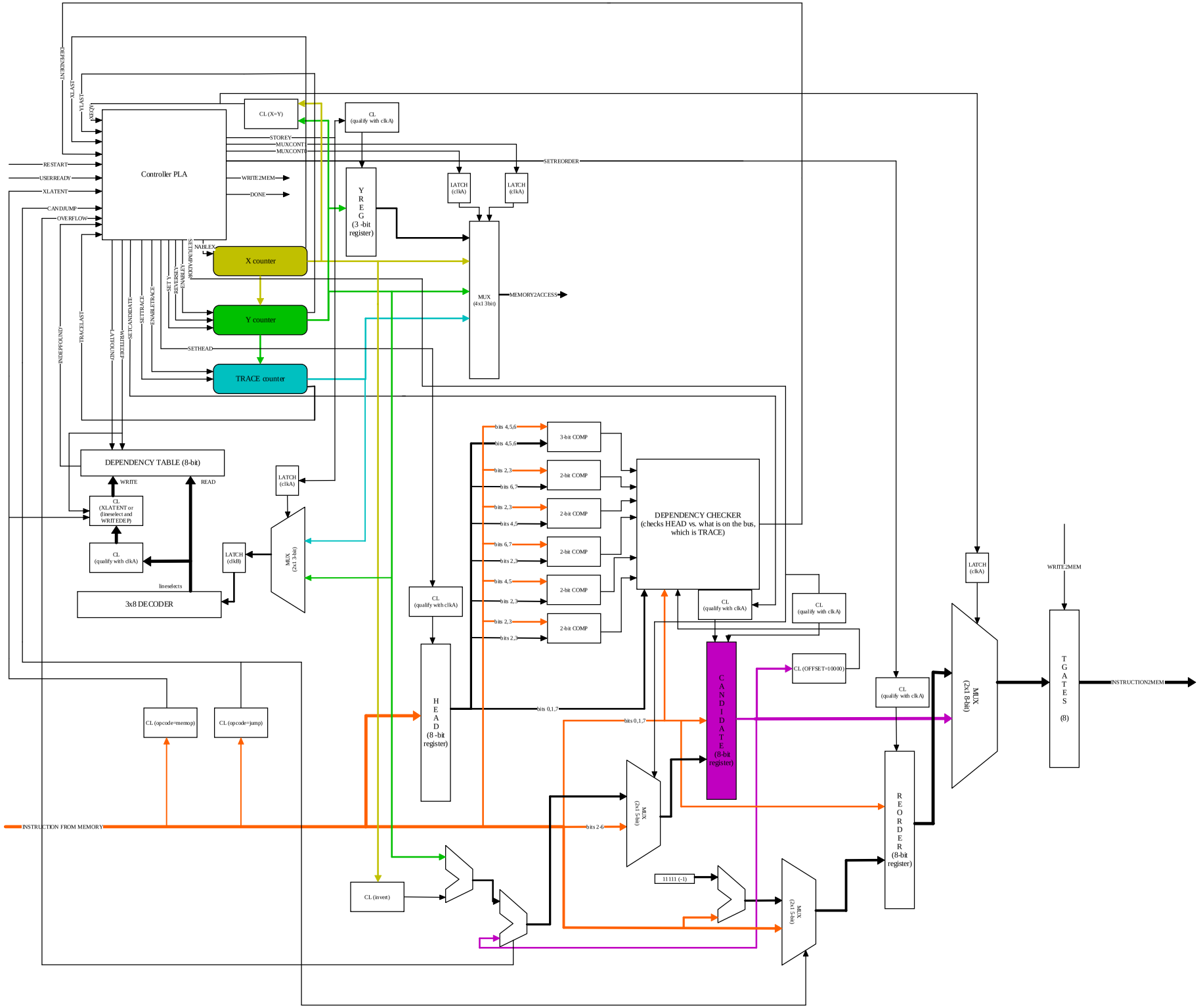
Controller PLA
RESTART
USERREADY
XLATENT
CANDJUMP
OVERFLOW
DEPENDENT
XLAST
YLAST
INDEX
CL (X=Y)
CL (qualify with clkA)
STOREY
MUXCONT
MUXCONT
SETREORDER
WRITE2MEM
DONE
Y R E G (3 -bit register)
LATCH (clkA)
LATCH (clkA)
NABLEX
X counter
Y counter
TRACE counter
SETY
REVERSEY
ENABLEY
DERIVEDPOINTERS
ENABLETRACE
SETTRACE
SETCANDDATE
WRITEDEP
LATFOUND
TRACELAST
INDEPFOUND
SETHEAD
MUX (4x1 3bit)
MEMORY2ACCESS
DEPENDENCY TABLE (8-bit)
WRITE
READ
CL (XLATENT or (lineselect and WRITEDEP)
CL (qualify with clkA)
lineselects
3x8 DECODER
LATCH (clkB)
LATCH (clkA)
MUX (2x1 3-bit)
bits 4,5,6
bits 4,5,6
bits 2,3
bits 6,7
bits 2,3
bits 4,5
bits 6,7
bits 2,3
bits 4,5
bits 2,3
bits 2,3
bits 2,3
3-bit COMP
2-bit COMP
2-bit COMP
2-bit COMP
2-bit COMP
2-bit COMP
DEPENDENCY CHECKER (checks HEAD vs. what is on the bus, which is TRACE)
CL (qualify with clkA)
CL (qualify with clkA)
CL (qualify with clkA)
CL (qualify with clkA)
H E A D (8 -bit register)
bits 0,1,7
bits 0,1,7
C A N D I D A T E (8-bit register)
CL (OFFSET=100000)
CL (qualify with clkA)
LATCH (clkA)
MUX (2x1 8-bit)
WRITE2MEM
T G A T E S (8)
INSTRUCTION2MEM
CL (opcode=memop)
CL (opcode=jump)
INSTRUCTION FROM MEMORY
bits 2-6
MUX (2x1 5-bit)
11111 (-1)
MUX (2x1 5-bit)
R E O R D E R (8-bit register)
CL (invert)